Amendments to the Claims:

Listing of Claims:

Claim 1 (original) A microcomputer apparatus comprising:

a processing unit for executing instructions; and

a loop counter coupled to the processing unit for receiving and storing a loop count value according to a loop instruction executed by the processing unit;

wherein the processing unit decrements the loop count value stored in the loop counter each time an instruction is looped, and when the processing unit encounters a loop instruction, the processing unit will loop the instruction previous to the loop instruction a number of times as defined by the loop count value.

Claim 2 (original) The microcomputer apparatus in claim 1 further comprising:

a first memory coupled to the processing unit for storing a program comprising a table containing the addresses of a plurality of loop count values.

Claim 3 (currently amended) The microcomputer apparatus in claim 2 wherein the ~~third~~ first memory is a ROM (Read Only Memory) memory.

Claim 4 (currently amended) The microcomputer apparatus in claim 2 further comprising:

a program counter coupled to the processing unit for addressing the ~~third~~ first memory.

Claim 5 (original) The microcomputer apparatus in claim 1 wherein the processing unit comprises:

an instruction decoding means for decoding and dispatching instructions for execution and for checking a loop count value stored in the loop counter; and

an execution unit for executing the dispatched instructions and decrementing a loop count value stored in the loop counter.

Claim 6 (original) The microcomputer apparatus in claim 1 wherein the loop counter comprises:

a first multiplexer for selecting an address of a loop count value,

a second multiplexer for determining whether a loop count value is being sent from the processing unit or from the address of a loop count value; and

a fourth memory for storing a loop count value and issuing the current state of the loop count value to the processing unit; wherein the processing unit will decrement the loop count value each time an instruction has been looped and will continue looping the instruction until the loop count value has reached 0.

Claim 7 (original) The microcomputer apparatus in claim 6 wherein the fourth memory is a loop count register.

Claim 8 (original) The microcomputer apparatus in claim 1 wherein the computer apparatus further comprises a storage unit coupled to the processing unit and the loop counter.

Claim 9 (original) The microcomputer apparatus in claim 8 wherein the storage unit further comprises:

a second memory coupled to the processing unit and the loop counter for storing a table containing the addresses of a plurality of loop count values; and

a third memory coupled to the loop counter for storing a plurality of loop count values.

Claim 10 (currently amended) The microcomputer apparatus in claim 9 wherein the ~~first~~ third memory is a set of registers.

Claim 11 (original) The microcomputer apparatus in claim 9 wherein the second memory is a RAM (Random Access Memory) memory.

Claim 12 (new) A microcomputer apparatus comprising:

a processing unit for executing instructions;

a second memory, coupled to the processing unit, for storing a table containing addresses of a plurality of loop count values;

a third memory, for storing the plurality of loop count values; and

a loop counter, coupled to the processing unit, the second memory and the third memory, for receiving and storing a loop count value from the third memory by an address read from the second memory according to a loop instruction executed by the processing unit;

wherein the processing unit will loop a target instruction corresponding to the loop instruction a number of times as defined by the loop count value.

Claim 13 (new) The microcomputer apparatus of claim 12 further comprising:

a first memory, coupled to the processing unit, for storing a program comprising the table containing the addresses of the plurality of loop count values;

wherein the second memory loads the table containing the addresses of the plurality of loop count values from the first memory.

Claim 14 (new) The microcomputer apparatus of claim 12 wherein the target instruction is previous to the loop instruction.